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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/604,381	07/16/2003	Pao-Ching Tseng	MTKP0048USA	1380
27765	7590	09/12/2006	EXAMINER	
NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION P.O. BOX 506 MERRIFIELD, VA 22116			PATEL, KAUSHIKKUMAR M	
			ART UNIT	PAPER NUMBER
			2188	

DATE MAILED: 09/12/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	10/604,381		TSENG ET AL.	
	Examiner		Art Unit	
	Kaushikkumar Patel		2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-8 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-8 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 16 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. This Office Action is in response to applicant's communication filed June 26, 2006 in response to PTO Office Action mailed April 18, 2006. The Applicant's remarks and amendments to the claims and/or specification were considered with the results that follow.
2. In response to the last Office Action, claims 2 and 8 have been amended. No new claims have been added. As a result, claims 1-8 remain pending in this application.
3. Objections to claims have been withdrawn due to amendment filed on June 26, 2006.

Response to Arguments

4. Applicant's arguments with respect to claims 1-8 have been considered but are not persuasive. Applicant argues that the memory bank selector is a hardware device (response to claim rejections, page 7), it is not mentioned anywhere in the specification that "the memory bank selector" is a hardware device, and hence the space selection instruction taught by Zhou can be interpreted as memory bank selector of the applicant. Applicant further argues that Zhou teaches a stack in data space and does not teach microprocessor comprising a stack. A definition of stack (The authoritative Dictionary of IEEE Standards Terms, page 1093), suggests that "the items are appended to and retrieved from the same end of list" and definition of stack architecture suggests use of such data structure. Further according to MPEP § 2111.02, "if the body of a claim fully

Art Unit: 2188

and intrinsically sets forth all of the limitations of the claimed invention, and preamble merely states, for example, the purpose (method) or intended use of the invention, rather than any distinct definition of any claimed invention's limitations, then the preamble is not considered a limitation and is of no significance to claim construction". Here the stack is used to keep track of a program's internal operations, and such a purpose is fulfilled by the data structure comprising a stack of Zhou. Applicant further argues that Zhou does not teach pushing a bank number of the current memory bank onto stack (response to claim rejections, page 8). Examiner respectfully disagrees with this. As per Zhou, col. 6, lines 65-66, "microprocessor saves the next address aaa1 on a stack" clearly suggest pushing the address to stack after an interrupt. The saving of address onto stack is meant as pushing the address onto stack because as explained above the stack inherently works by pushing and popping the data from stack (see attached definitions from Google, pages 1-3). Applicant further argues that Zhou does not teach popping the bank address. As per Zhou, col. 7, lines 7-10, "microprocessor resumes execution, for example, retrieves the next instruction from address aaa1 popped from the stack". With regard to claims 2 and 8, applicant argues that "z80" is not a microcontroller-based processor. A definition and brief search on Google proves that "z80" is a microcontroller series microprocessor. Accordingly, the rejection of claims are maintained and reiterated below for applicant's convenience.

Drawings

5. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: The amendment filed to specification on June 26, 2006 contains the reference numbers that are not present in any drawing. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

7. Claims 1-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Zhou et al. (5,913,924) (Zhou herein after).

As per claim 1, Zhou teaches a method for accessing a memory having a storage space larger than the addressing capacity of a microprocessor (abstract, figs. 4-5), the memory comprising a plurality of memory banks (fig. 1), the microprocessor comprising a stack (column 6, line 66), an interrupt processing unit, and a memory bank selector for selecting the memory banks (column 6, lines 49-55), the method comprising:

(a) storing an interrupt service routine in one of the memory banks (column 6, lines 50-52);

(b) when an interrupt occurs, pushing a current program counter address onto the stack by the interrupt processing unit, pushing a bank number of the current memory bank onto the stack, and setting the memory bank selector to the bank number of the memory bank storing the interrupt service routine (column 6, lines 65-67, column 7, lines 10-37);

(c) switching the microprocessor to the memory bank storing the interrupt service routine to execute the interrupt service routine (column 7, lines 25-35, only memory bank 370 A stores interrupt service routine, and during program execution in bank 370B, after interrupt switches to bank 370A for interrupt service routine);

(d) after interrupt service routine finishes execution, popping the bank number of the memory bank stored in the step (b) from the stack by the interrupt processor unit, restoring the popped bank number to the memory bank selector, and popping program counter address stored in the stack in step (b) from the stack (column 7, lines 6-9, lines 41-59);

Art Unit: 2188

(e) switching the microprocessor back to the memory bank corresponding to the bank number stored in the memory bank selector to continue executing the program interrupted in step (b) (column 7, lines 55-59).

As per claim 2, Zhou teaches microprocessor is Microcontroller series processor (column 4, line 39).

As per claim 3, Zhou teaches common area in each memory bank (fig. 3, items 375A and 375B).

As per claim 4, Zhou teaches memory banks storing interrupt service routine in only in one memory bank separate from bank selection routine (column 7, lines 60-67).

As per claim 5, Zhou teaches single chip microprocessor (fig.3, item 310).

Claims 6-8 are also rejected under same rationales as applied to claims 1-5 above, as Zhou teaches a device (computer system, see abstract), with microprocessor and plurality of memory banks as applied to claims 1-5 above.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Bjerge et al. (5,655,099) teaches bank switching access program instructions stored in one memory bank.

Kaneko (5,146,581) teaches multiple memory banks storing interrupt service routines for bank switching.

Ma et al. (US 6,691,219) teaches extending memory address range and interrupt processing in multi-bank memories.

Takiguchi et al. (5,557,766) teaches bank-structured memories capable of handling multiple interrupts.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kaushikkumar Patel whose telephone number is 571-272-5536. The examiner can normally be reached on 8.00 am - 4.30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on 571-272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

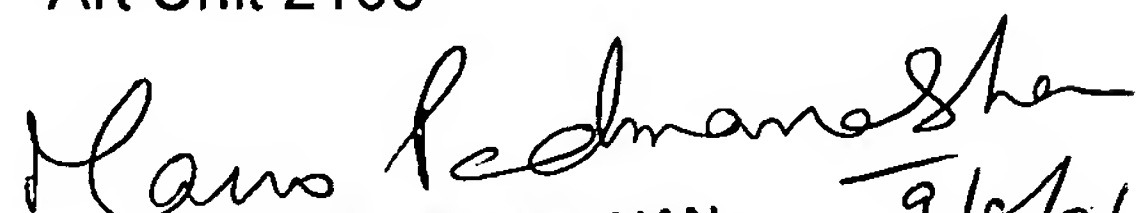
Art Unit: 2188

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



kmp

Kaushikkumar Patel
Examiner
Art Unit 2188



MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER 9/8/06